FAIRCHILD SEMICONDUCTOR®

May 2008

FAN5110 — Two-Phase, Bootstrapped, 12V NMOSFET Half-Bridge Driver

Features

- Two-phase, N-channel MOSFET driver in a Single Compact Package for Multi-phase Buck Converter Applications
- Each Phase Drives the N-channel High-side and Low-side MOSFETs in a Synchronous Buck Configuration
- Two-phase Driver Reduces Printed Circuit Board Area
- Variable High-side and Low-side Gate Drive Voltages for Flexibility and Performance Optimization at Higher Frequencies
- Internal Adaptive "Shoot-through" Protection
- Fast Rise and Fall Times
- High Switching Frequency: up to 1 MHz
- Common Enable (EN) Turns Off both Upper and Lower Output FETs
- TTL-compatible PWM and EN Inputs
- Under-Voltage Lockout Protection Feature
- Available in SOIC-16 and MLP-16 Packages

Applications

- Multi-Phase VRM/VRD Regulators for Microprocessor Supplies
- Two Separate, Single-phase Supply Designs
- High-Current, High-Frequency DC/DC Converters
- High-Power Modular Supplies
- General-Purpose, TTL Input, 12V Driver for Half-Bridge and Full-Bridge Applications

Description

FAN5110 contains two N-channel MOSFET drivers on a single die in one package. It replaces two single-phase drivers in a multiple-phase PWM design. Each phase is specifically designed to drive both the upper and lower N-channel power MOSFETs of a synchronous rectified buck converter at high switching frequencies.

This two-phase driver, combined with a Fairchild multi-phase PWM controller and power MOSFETs, forms a complete V-core power supply solution for advanced microprocessors.

The lower drivers are powered externally through the PVCC pin. The PVCC pin is normally connected to V_{CC}, which drives the lower MOSFET's gates at $12V_{GS}$. Connecting the PVCC pin to a voltage lower than V_{CC} lowers the V_{GS} voltage, resulting in much less driver power dissipation. This is especially valuable when driving MOSFETs with high gate charge (Q_{gtot}) and in applications requiring high switching frequencies.

The driver's adaptive shoot-through protection prevents the upper and lower MOSFETs from conducting simultaneously. The FAN5110 is rated for operation from 0°C to +85°C and is available in a low-cost 16-pin (Small Outline Integrated Circuit) SOIC package and a higher power MLP-16 package.

Related Resources

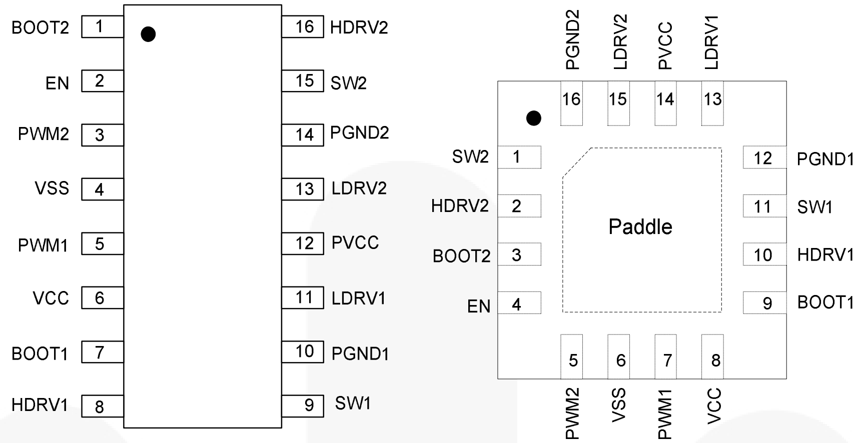
- *AN-6003 — "Shoot-through" in Synchronous Buck Converters*

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status	Packing Method	Quantity Per Reel
FAN5110MX	0°C to 85°C	SOIC-16	RoHS	Tape and Reel	2500
FAN5110MPX	0°C to 85°C	MLP-16, 4x4mm	RoHS	Tape and Reel	2500

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Pin Configurations



SOIC16 Package
Top View

MLP16 Package
Top View

Figure 1. Packages (Top View)

Pin Definitions

MLP	SOIC	Name	Description
1	15	**SW2**	**Switch Node Input**. Connect as shown in Figure 1. SW provides return for the high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
2	16	**HDRV2**	**High-Side Gate Drive Output**. Connect to the gate of the high-side power MOSFET(s).
3	1	**BOOT2**	**Bootstrap Supply Input**. Provides voltage supply to the high-side MOSFET driver. Connect to bootstrap capacitor and diode.
4	2	**EN**	**Enable**. When LOW, this pin disables FET switching (HDRV and LDRV are held LOW). This pin is common for both drivers *(previously referred to as OD#)*.
5	3	**PWM2**	**PWM Signal Input**. Accepts a logic-level PWM signal from the controller.
6	4	**VSS**	**Signal Ground**. Connect directly to the ground plane.
7	5	**PWM1**	**PWM Signal Input**. Accepts a logic-level PWM signal from the controller.
8	6	**VCC**	**Power Input Voltage**. +12V power for the internal logic. Bypass with a minimum 1µF X7R or 4.7µF X5R ceramic capacitor.
9	7	**BOOT1**	**Bootstrap Supply Input**. Provides voltage supply to the high-side MOSFET driver. Connect to bootstrap capacitor and diode.
10	8	**HDRV1**	**High Gate Drive Output**. Connect to the gate of the high-side power MOSFET(s).
11	9	**SW1**	**Switch Node Input**. Connect as shown in Figure 1. SW provides return for the high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
12	10	**PGND1**	**Power Ground**. Connect directly to the source of low-side MOSFET(s) and C_{VCC}.
13	11	**LDRV1**	**Low-Side Gate Drive Output**. Connect to the gate of the low-side power MOSFET(s).
14	12	**PVCC**	**Lower Gate Drive Voltage**. This is the input supply for the lower drivers. The V_{GS} of the lower MOSFETs matches this voltage. Connect to V_{CC} or a lower voltage.
15	13	**LDRV2**	**Lower Gate Drive Output**. Connect to the gate of the low-side power MOSFET(s).
16	14	**PGND2**	**Power Ground**. Connect directly to the source of low-side MOSFET(s) and C_{VCC}.
	NA	**Paddle**	**MLP Package Only.** Connected to ground inside the chip. Connect to ground plane for lowest thermal resistance.

Application Diagram

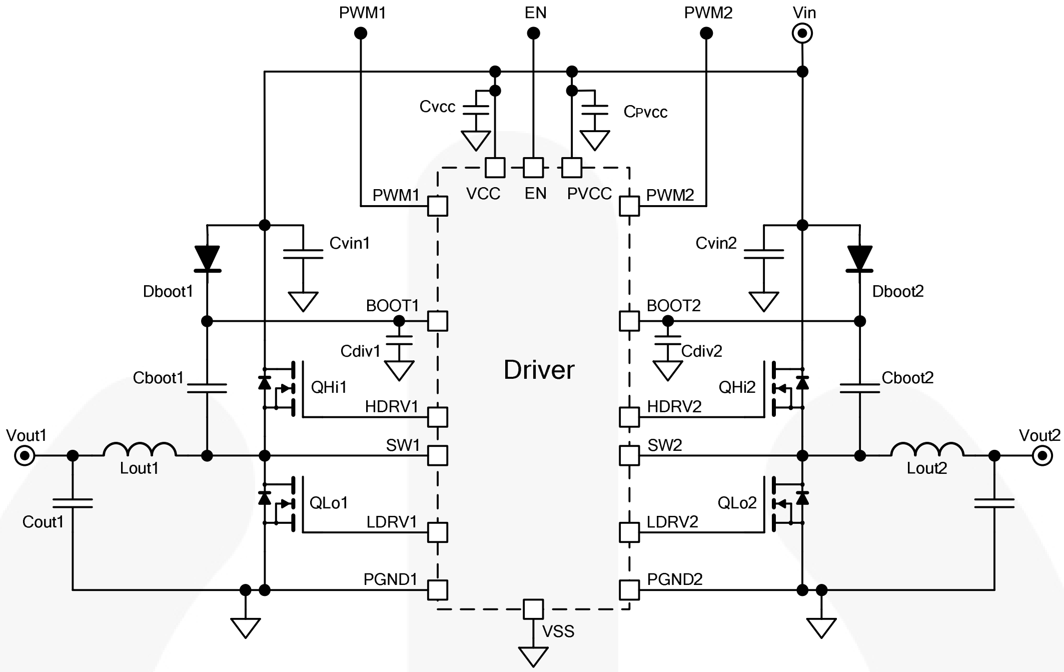


Figure 2. Typical Two-Phase Application

Block Diagram

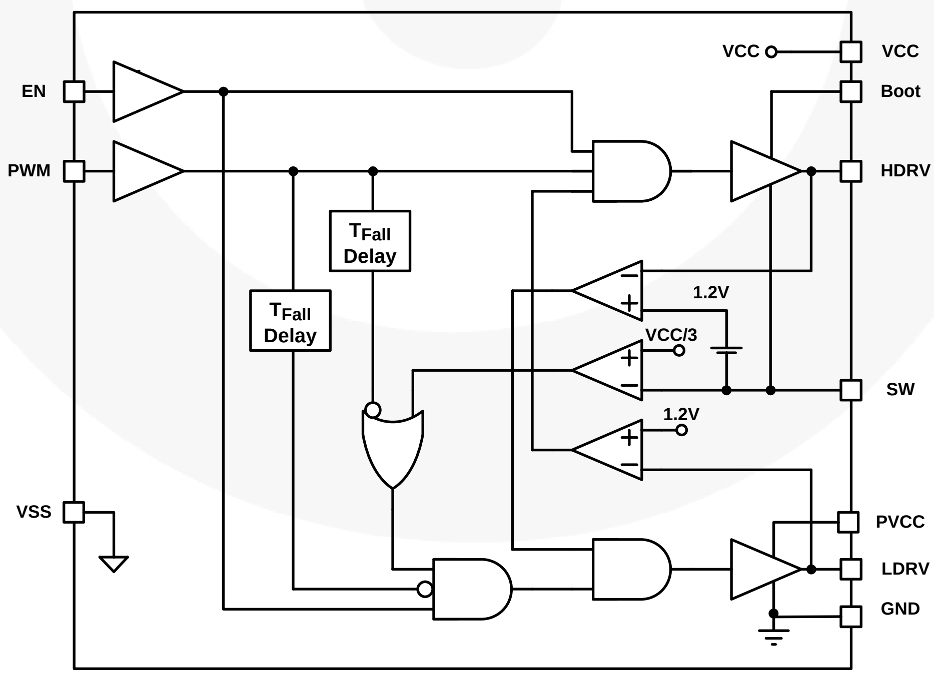


Figure 3. Functional Block Diagram, Each Side

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. Absolute maximum ratings are stress ratings only. Unless otherwise specified, voltages referenced to GND.

Parameter	Conditions	Min.	Max.	Unit
VCC and PVCC to GND	Continuous	-0.3	15.0	V
	Transient (t < 4ns)[1]	-0.3	19.0	V
PWM and EN Pins		-0.3	5.5	V
SW to GND	Continuous	-1	15	V
	Transient (t < 100ns)[1]	-5	25	V
BOOT to SW	Continuous	-0.3	15.0	V
	Transient (t < 20ns)	-2	17	V
BOOT to GND	Continuous	-0.3	30.0	V
	Transient (t < 100ns)[1]		38	V
HDRV		V_{SW} -1.0	V_{BOOT}+0.3	V
LDRV	Continuous	-0.5	V_{CC}	V
	Transient (t < 200ns)[1]	-2.0	V_{CC}+0.3	V
	Transient (t < 20ns)	-2.0	V_{CC}+2.0	V

Note:
1. For transient derating beyond the levels indicated, refer to Figure 17 and Figure 18.

Thermal Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature	0		+150	°C
T_{STG}	Storage Temperature	-65		+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+300	°C
T_{VP}	Vapor Phase, 60 Seconds			+215	°C
T_{LI}	Infrared, 15 Seconds			+220	°C
P_D	Power Dissipation, T_A = 25°C, T_{JMAX} = 125°C			850	mW
θ_{JC}	Thermal Resistance, SO-16, Junction-to-Board		40		°C/W
θ_{JA}	Thermal Resistance, SO-16, Junction-to-Ambient		117		°C/W
θ_{JC}	Thermal Resistance, MLP16, Junction-to-Case		5		°C/W
θ_{JA}	Thermal Resistance, MLP16, Junction-to-Ambient		37		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	V_{CC} to Ground	10.0	12.0	13.5	V
PV_{CC}	PVCC Input Voltage	PV_{CC} to Ground	8.0	12.0	13.5	V
V_{IO}	Boot Diode Anode Voltage	Anode to Ground	8.0	12.0	13.5	V
T_A	Ambient Temperature		0		+85	°C
T_J	Junction Temperature		0		+125	°C

Electrical Characteristics

V_{CC} and P_{VCC} = 12V, and T_A = 25°C using the circuit in Figure 4 unless otherwise noted. The "•" denotes specifications that apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Input Supply							
V_{CC}	V_{CC} and P_{VCC} Voltage Range		•	6.4	12.0	13.5	V
I_{CC}	V_{CC} Current	EN = 0V	•		4.1	8.0	mA
V_{UYR}	V_{CC} Rising	1V/ms			4.7	5.3	V
V_{UVF}	V_{CC} Falling	1V/ms		3.4	4.2		V
V_{HYS}	V_{CC} Hysteresis			175	325		mV
EN Input							
$V_{IH(EN)}$	Input High Voltage		•	2.0			V
$V_{IL(EN)}$	Input Low Voltage		•			0.8	V
$V_{HYS(EN)}$	Input Hysteresis		•		550		mV
I_{EN}	Input Current	EN = 3.0V	•	-300		+300	nA
$t_{pdl(EN)}$	Propagation Delay(3)	Figure 5			25	40	ns
$t_{pdh(EN)}$					15	30	ns
PWM Input							
$V_{IH(PWM)}$	Input High Voltage		•	2.0			V
$V_{IL(PWM)}$	Input Low Voltage		•			0.8	V
$V_{HYS(PWM)}$	Input Hysteresis		•		550		mV
$I_{IL(PWM)}$	Input Current		•	-1		+1	μA
SW Pin							
R_{SW}	SW Pin Bleeder	EN = 0V, V_{SW} = 4.0V	•	700	1000	1300	Ω
High-Side Driver							
R_{HUP}	Output Resistance, Sourcing	$V_{BOOT} - V_{SW}$ = 12V			2.5	3.3	Ω
$I_{SOURCE(LDRV)}$	Source Current(3)	V_{DS} = -10V			2.0		A
R_{HDN}	Output Resistance, Sinking	$V_{BOOT} - V_{SW}$ = 12V			1.1	1.4	Ω
$I_{SINK(HDRV)}$	Sink Current(3)	V_{DS} = 10V			2.7		A
$t_{R(HDRV)}$	Transition Times(3, 5)	Figure 4			30	45	ns
$t_{F(HDRV)}$					25	30	ns
$t_{pdh(HDRV)}$	Propagation Delay(3, 4)	Figure 6			35	50	ns
$t_{pdl(HDRV)}$					25	40	ns

Continued on the following page…

Electrical Characteristics (Continued)

V_{CC} and P_{VCC} = 12V, and T_A = 25°C using the circuit in Figure 4 unless otherwise noted. The "•" denotes specifications that apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Low-Side Driver							
PVCC	PVCC Voltage Range			6.4	12.0	13.5	V
R_{LUP}	Output Resistance, Sourcing				2.0	2.3	Ω
$I_{SOURCE(LDRV)}$	Source Current[3]	V_{DS} = -10V			2.7		A
R_{LDN}	Output Resistance, Sinking				1.0	1.3	Ω
$I_{SINK(LDRV)}$	Sink Current[3]	V_{DS} = 10V			3.5		A
BG_{th}	Bottom Gate Threshold			1.0	1.3	1.6	V
BG_{hys}	Bottom Gate Hysteresis			0.5	0.8		V
$t_{R(LDRV)}$	Transition Times[3, 5]	Figure 4			25	35	ns
$t_{F(LDRV)}$					20	30	ns
$t_{pdh(LDRV)}$	Propagation Delay[3, 4]	Figure 6			20	30	ns
$t_{pdl(LDRV)}$					15	20	ns
$t_{pdh(LDF)}$		See *Adaptive Gate Drive Circuit Description*			170		ns

Notes:
2. Limits at operating temperature extremes are guaranteed by design, characterization, and statistical quality control.
3. Specifications guaranteed by design and characterization (not production tested).
4. For propagation delays, t_{pdh} refers to low-to-high signal transition. t_{pdl} refers to high-to-low signal transition.
5. Transition times are defined for 10% and 90% of DC values.

Test Diagrams

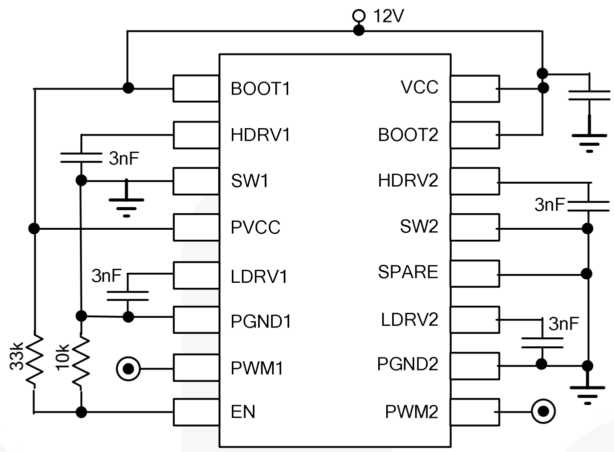


Figure 4. Test Circuit

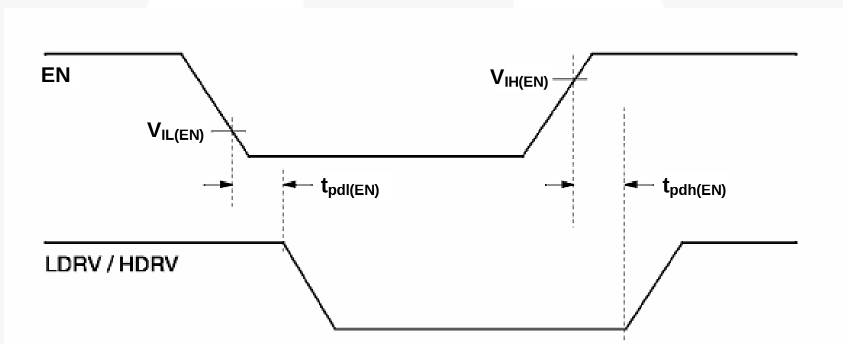


Figure 5. Enable Timing

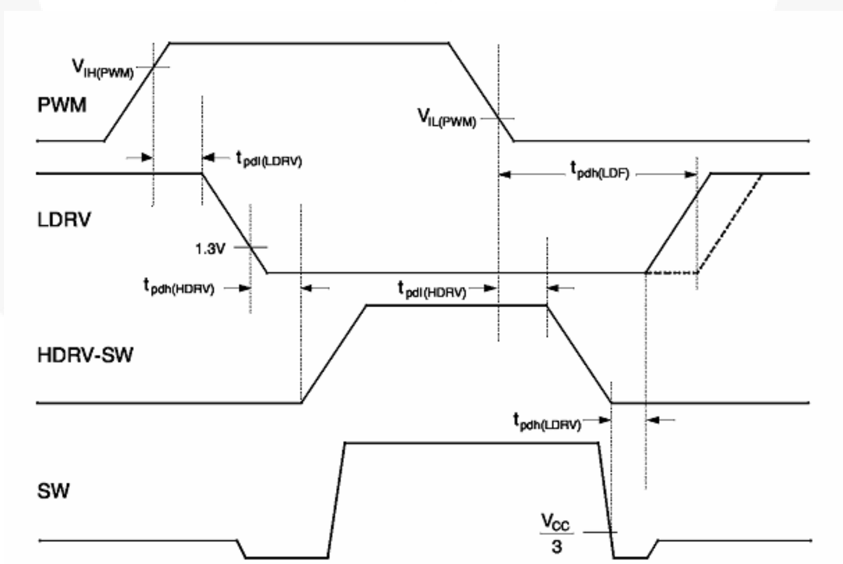


Figure 6. Adaptive Gate Drive Timing

Typical Performance Characteristics

Performance characteristics achieved using the test circuit shown in Figure 4.

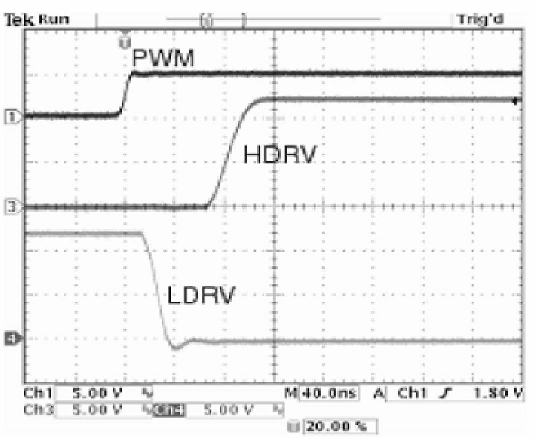


Figure 7. PWM Rise Time Waveforms

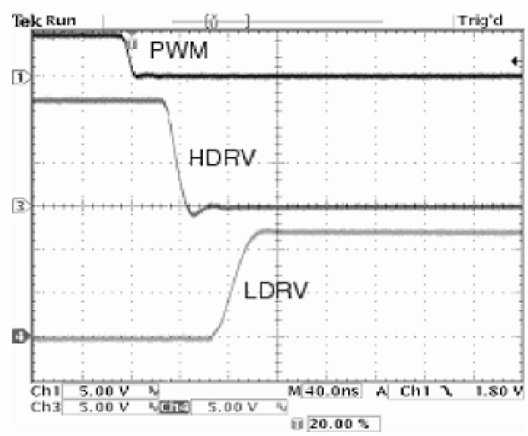


Figure 8. PWM Fall Time Waveforms

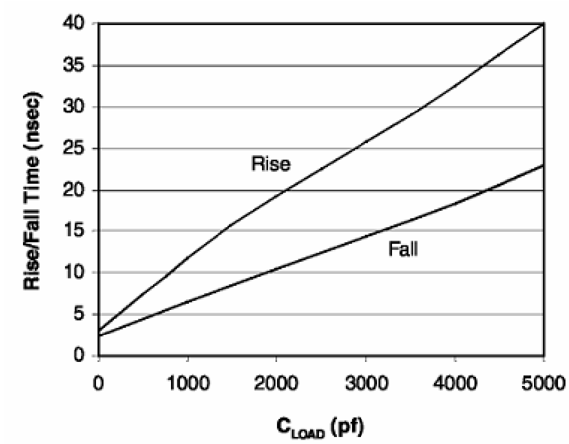


Figure 9. HDRV Rise and Fall Times vs. C_{LOAD}

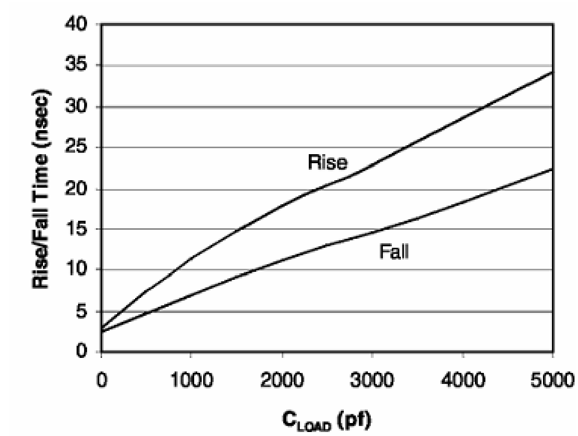


Figure 10. LDRV Rise and Fall Times vs. C_{LOAD}

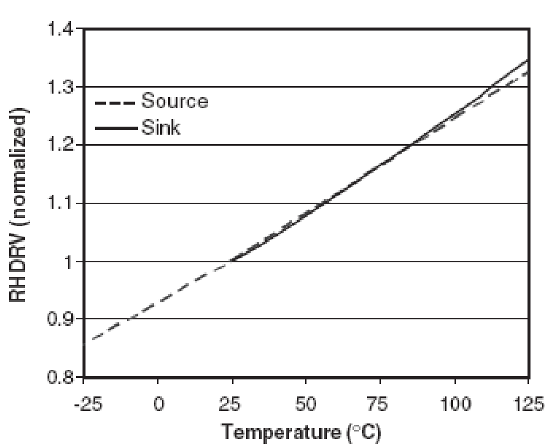


Figure 11. HDRV Resistance vs. Temperature

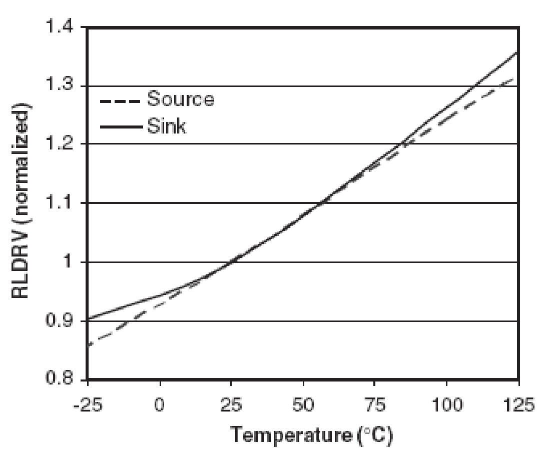


Figure 12. LDRV Resistance vs. Temperature

Typical Performance Characteristics (Continued)

Performance characteristics achieved using the test circuit shown in Figure 4.

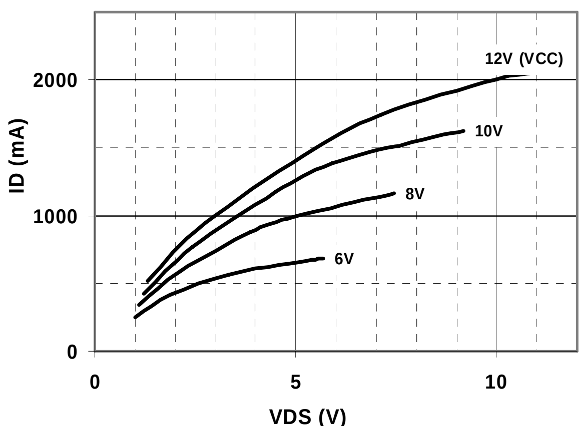


Figure 13. HDRV Pull-Up (Sourcing)

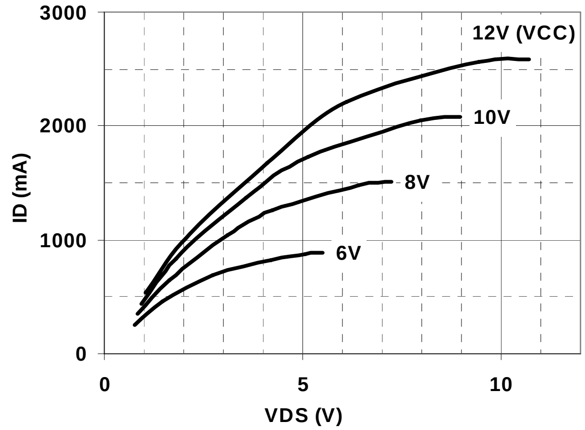


Figure 14. LDRV Pull-Up (Sourcing)

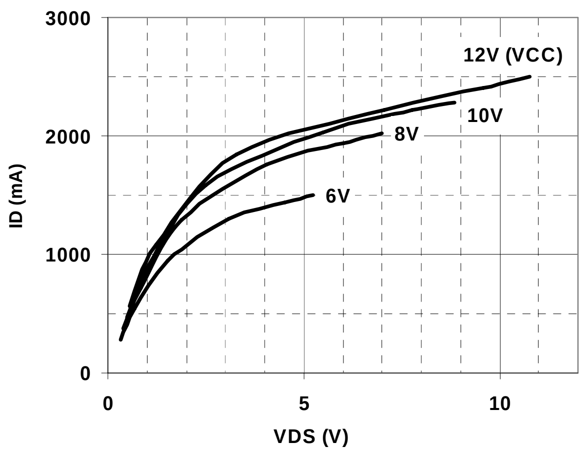


Figure 15. HDRV Pull-Down (Sinking)

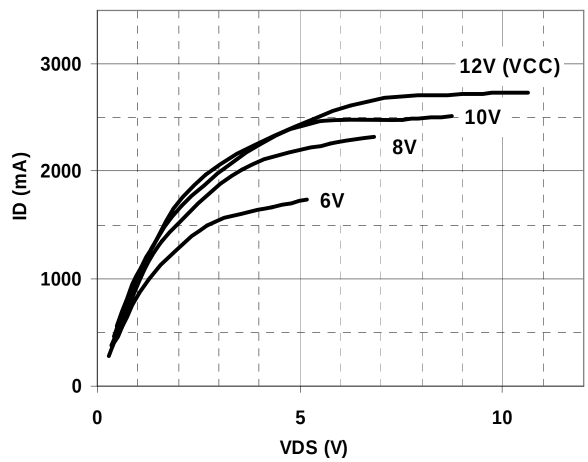


Figure 16. LDRV Pull-Down (Sinking)

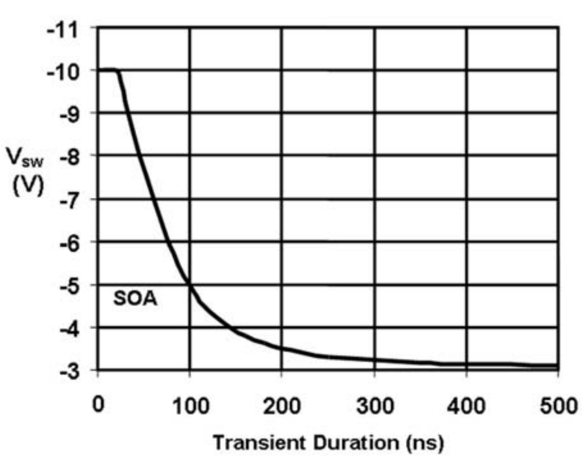


Figure 17. Negative SW Voltage Transient

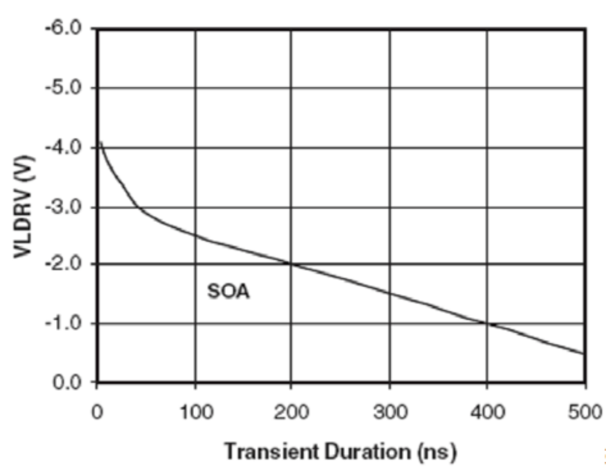


Figure 18. Negative LDRV Voltage Transient

Typical Performance Characteristics (Continued)

Performance characteristics below were achieved using a modified version of the test circuit shown in Figure 4. The BOOT and PVCC pins were disconnected from V_{CC}; a boot diode was connected in series with the BOOT pin; and the PVCC and boot diode anode were connected to a variable voltage power supply. V_{CC} was held constant at 12V during the test.

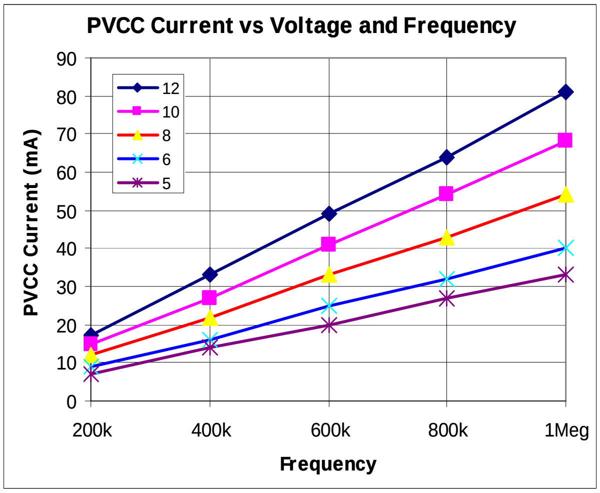


Figure 19. PV_{CC} Operating Current

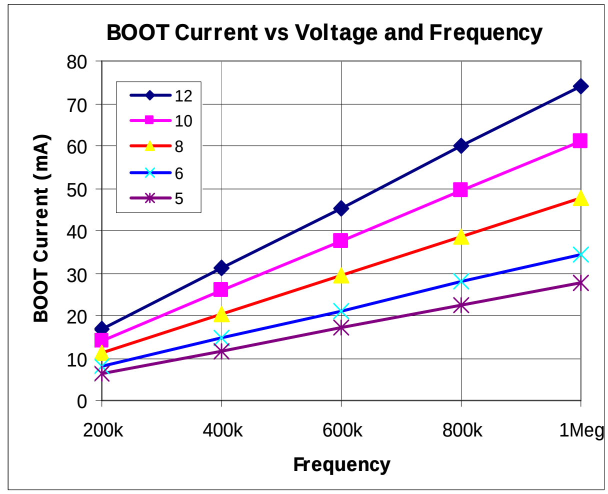


Figure 20. Boot Operating Current

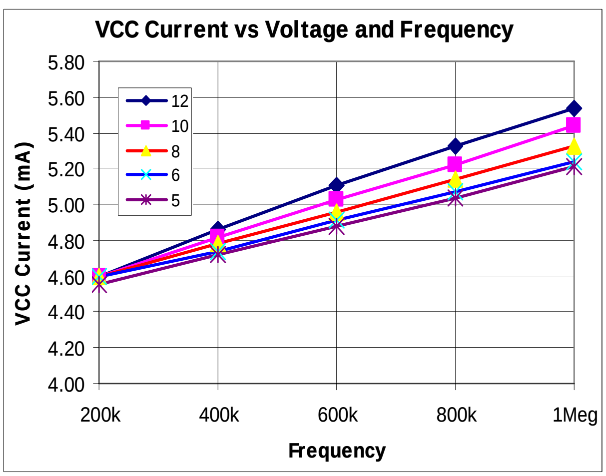


Figure 21. V_{CC} Operating Current

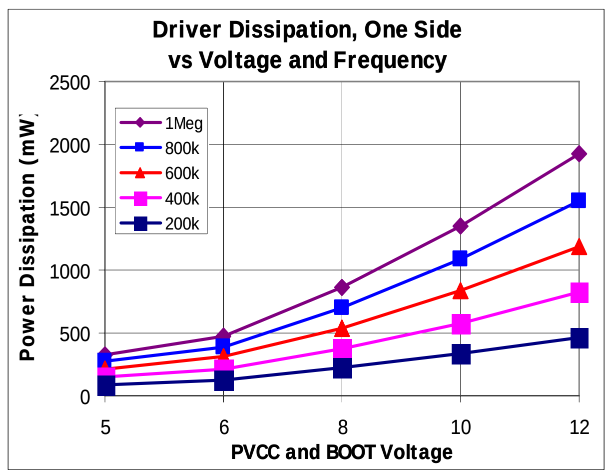


Figure 22. Driver Power Dissipation, One Side

Circuit Description

The FAN5110 contains two half-bridge MOSFET drivers in a single 16-pin package. Each driver is optimized for driving N-channel MOSFETs in a synchronous buck converter topology. Each driver's TTL-compatible PWM input signal is all that is required to properly drive the high-side and low-side MOSFETs. The following sections apply to each driver.

Low-Side Driver

The low-side driver (LDRV) is designed to drive ground-referenced, low-$R_{DS(on)}$, N-channel MOSFETs. The power for LDRV is internally connected to the PVCC pin. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the FAN5110 is disabled (EN = 0V), LDRV is held low.

High-Side Driver

The FAN5110's high-side driver (HDRV) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of an external diode and bootstrap capacitor (C_{BOOT}).

During start-up, SW is held at GND, allowing C_{BOOT} to charge to V_{CC} through the diode. When the PWM input goes high, HDRV begins to charge the high-side MOSFET gate (QHi). During this transition, charge is transferred from C_{BOOT} to QHi's gate. As QHi turns on, SW rises to V_{IN}, forcing the BOOT pin to V_{IN} + $V_{C(BOOT)}$, which provides sufficient V_{GS} enhancement for QHi. To complete the switching cycle, QHi is turned off by pulling HDRV to SW. C_{BOOT} is recharged to V_{CC} when SW falls to GND. HDRV output is in phase with PWM input. When the driver is disabled, the high-side gate is held low.

Adaptive Gate Drive Circuit

The FAN5110 embodies an advanced design that ensures minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive, adaptively, to ensure they do not conduct simultaneously. Refer to the gate drive rise and fall time waveforms shown in Figure 7 and Figure 8 for the relevant timing information.

To prevent overlap during the low-to-high switching transition (QLo OFF to QLo ON), the adaptive circuitry monitors the voltage at the LDRV pin. When the PWM signal goes HIGH, QHi begins to turn OFF after a propagation delay, as defined by the $t_{pdl(LDRV)}$ parameter. Once the LDRV pin is discharged below ~1.3V, QHi begins to turn ON after adaptive delay $t_{pdh(HDRV)}$.

To preclude overlap during the high-to-low transition (QLo OFF to QHi ON), the adaptive circuitry monitors the voltage at the SW pin. When the PWM signal goes LOW, QLo begins to turn OFF after a propagation delay ($t_{pdl(HDRV)}$). Once the SW pin falls below V_{CC}/3, QHi begins to turn ON after adaptive delay $t_{pdh(LDRV)}$.

V_{GS} of QLo is also monitored. When $V_{GS(QLo)}$ is discharged below ~1.3V, a secondary adaptive delay is initiated, which results in QHi being driven ON after $t_{pdh(LDF)}$, regardless of the SW state. This function is implemented to ensure that C_{BOOT} is recharged after each switching cycle, particularly for cases where the power converter is sinking current and the SW voltage does not fall below the V_{CC}/3 adaptive threshold. The secondary delay $t_{pdh(LDF)}$ is longer than $t_{pdh(LDRV)}$.

Application Information

Supply Capacitor Selection

For the supply input (V_{CC}), a local ceramic bypass capacitor is recommended to reduce the noise and to supply the peak current. Use at least a 1µF, X7R or X5R capacitor, close to the VCC and PGND pins. A 1µF bypass capacitor should be connected at the PVCC pin to PGND.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}) and an external diode, as shown in Figure 2. These components should be selected after the high-side MOSFET has been chosen. The required capacitance is determined using the following equation:

$$C_{BOOT} = \frac{Q_G}{\Delta V_{BOOT}} \quad (1)$$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BOOT} is the voltage droop allowed on the high-side MOSFET drive. For example, the Q_G of the FDD6696 MOSFET is about 35nC at $12V_{GS}$. For an allowed droop of ~300mV, the required bootstrap capacitance is 100nF. A good quality ceramic capacitor must be used.

The average diode forward current, $I_{F(AVG)}$, can be estimated by:

$$I_{f(AVG)} = Q_{GATE} \times f_{SW} \quad (2)$$

where f_{SW} is the switching frequency of the controller.

The peak surge current rating of the diode should be checked in-circuit, since this is dependent on the equivalent impedance of the entire bootstrap circuit, including the PCB traces.

Thermal Considerations

The total device dissipation is the total of both phases.

Device dissipation for a phase can be calculated as:

$$P_{Dtot} = P_Q + P_{HDRV} + P_{LDRV} \quad (3)$$

where:
P_Q represents quiescent power dissipation:

$$P_Q = V_{CC} \times \left[4mA + 0.036\left(f_{SW} - 100\right)\right] \quad (4)$$

f_{SW} is switching frequency (in kHz).

P_{HDRV} represents the power dissipation of the upper FET driver.

P_{LDRV} is dissipation of the lower FET driver.

Calculation of P_{HDRV}:

$$P_{QH} = \tfrac{1}{2} \times Q_{GH} \times V_{GS(Q1)} \times f_{SW} \quad (5)$$

$$P_{HDRV} = P_{H(R)} + P_{H(F)} \quad (6)$$

$$P_{H(R)} = P_{QH} \times \frac{R_{HUP}}{R_{HUP} + R_E + R_G} \quad (7)$$

$$P_{H(F)} = P_{QH} \times \frac{R_{HDN}}{R_{HUP} + R_E + R_G} \quad (8)$$

where:
$P_{H(R)}$ and $P_{H(F)}$ are dissipations for the rising and falling edges, respectively.

Q_{GH} is total gate charge of the upper FET for its applied V_{GS}.

As described in Equations 6 and 7, the total power dissapated in driving the gate is divided in proportion to the resistances in series with the MOSFET internal gate node, as shown in Figure 23.

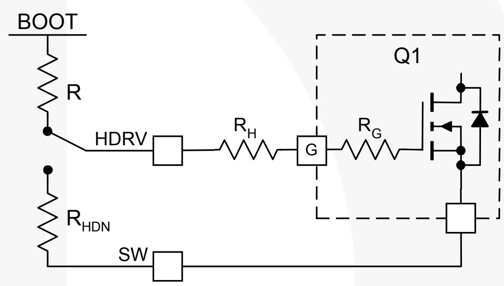


Figure 23. Driver Dissipation Model

R_G is the gate resistance internal to the FET. R_E is the external gate drive resistor implemented in many designs. Note that the introduction of R_E can reduce driver power dissipation, but excess R_E may cause errors in the "adaptive gate drive" circuitry. In particular, adding R_E in the low drive circuit could result in shoot-through. For more information, refer to *Application Note AN-6003, "Shoot-through" in Synchronous Buck Converters*.

Calculation of PLDRV:

$$P_{QH} = \tfrac{1}{2} \times Q_{GH} \times V_{GS(Q1)} \times f_{SW} \quad (9)$$

$$P_{LDRV} = P_{L(R)} + P_{L(F)} \quad (10)$$

$$P_{L(R)} = P_{QL} \times \frac{R_{LUP}}{R_{LUP} + R_E + R_G} \quad (11)$$

$$P_{L(F)} = P_{QL} \times \frac{R_{LDN}}{R_{HDN} + R_E + R_G} \quad (12)$$

where:
$P_{L(R)}$ and $P_{L(F)}$ are internal dissipations for the rising and falling edges, respectively.

Q_{GL} is total gate charge of the lower FET for its applied V_{GS}.

Layout Considerations

Use the following general guidelines when designing printed circuit boards *(see Figure 24)*:

- Trace out the high-current paths and use short, wide (>25 mil) traces to make these connections. If vias are required use multiple vias to lower the inductance.
- Connect the PGND pin as close as possible to the source of the lower MOSFET.
- The V_{CC} bypass capacitor must be located as close as possible to the VCC and VSS pins of the device. This is also true for the PV_{CC} bypass capacitor (PVCC and the PGND pins).
- Use multiple vias to other layers when possible to maximize the conduction of heat away from the package. This is particularly true for the paddle of the MLP package, which can be connected with vias to the internal ground plane of the board.

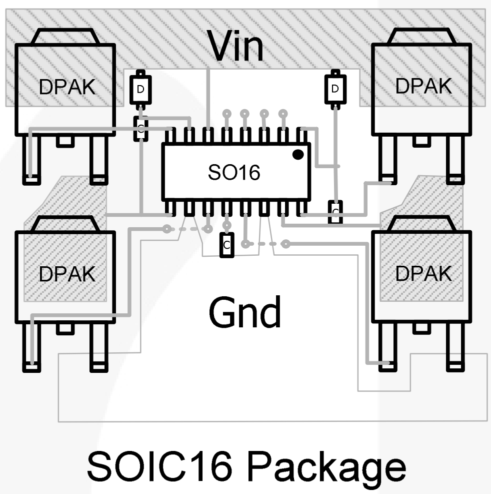


Figure 24. Recommended Layout Examples

Physical Dimensions

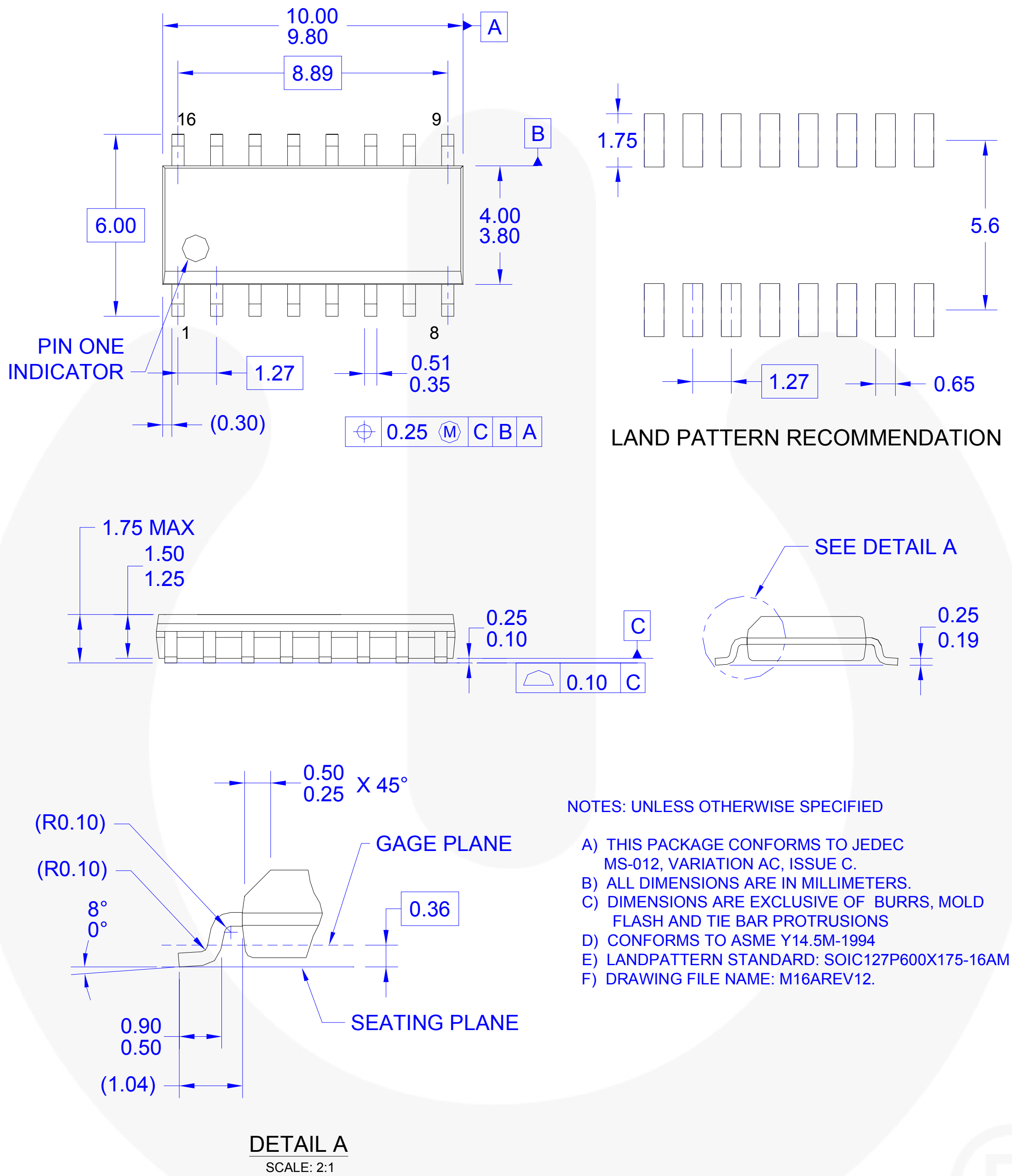


Figure 25. 16-Lead, Small Outline Integrated Circuit (SOIC) Package, 0.150 inches Narrow, JEDEC MS-012

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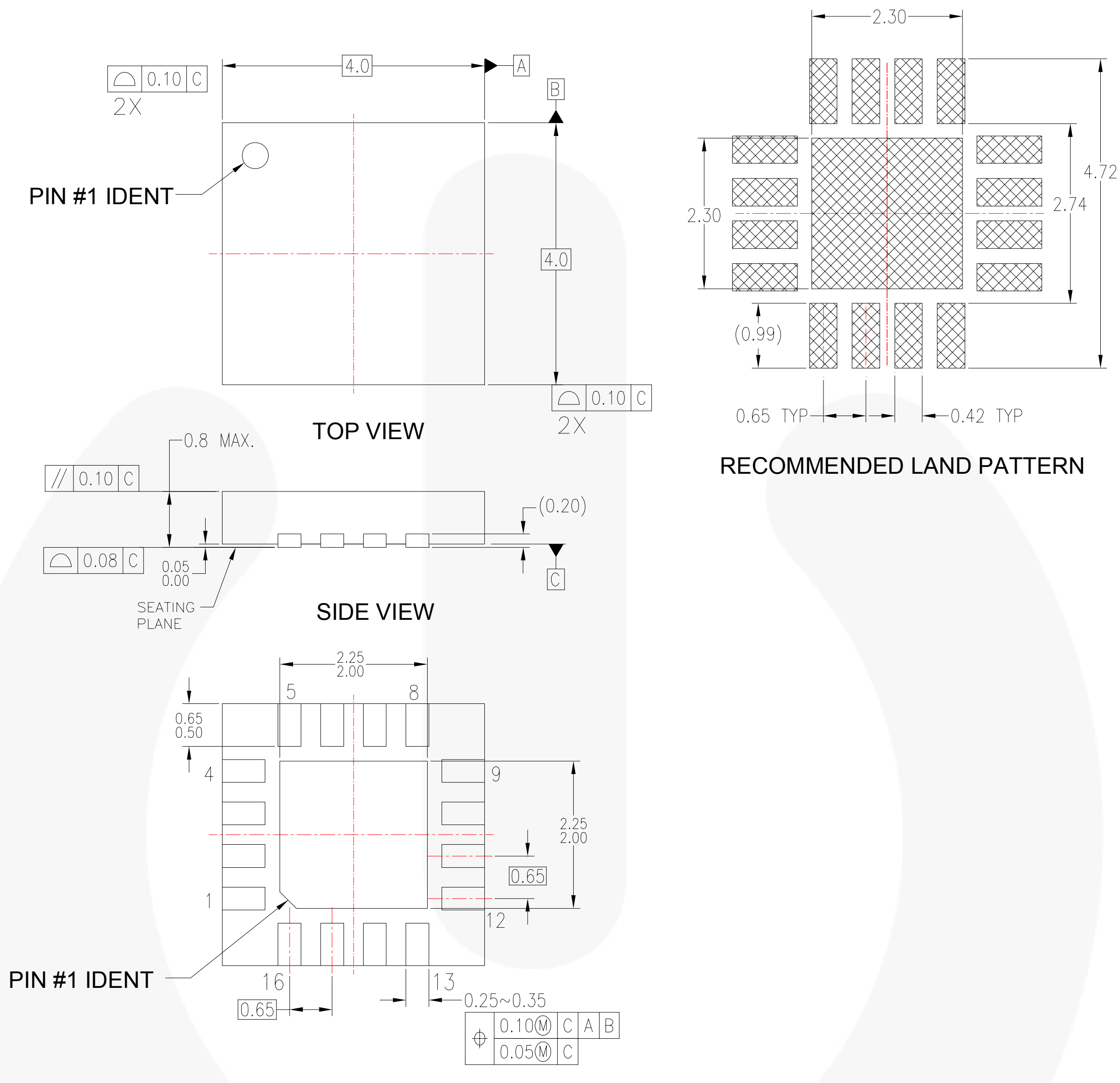
Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WGGC, DATED MAY/2005

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP16DrevB

Figure 26. 16 Lead MLP, JEDEC MO-220, 4mm Square

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